REMARKS

Claims 1-27 are pending and are rejected. Claims 1, 10, 20, 21, 25, 26 and 27 have been amended. Applicants gratefully acknowledge the Examiner's reconsideration and withdrawal of the previous anticipation rejections, and respectfully request reconsideration of the current claim rejections based on the above amendments and following remarks.

Claim Rejections Under 35 U.S.C. §102

Claims 1-6, 10-15, 20-21 and 25-27 are rejected as being anticipated by U.S. Patent No. 5,935,428 to Yamamoto Applicants respectfully submit that at the very least, claims 1, 10, 20, 21 and 25-27 are patentably distinct and patentable over Yamamoto.

On a fundamental level, Yamamoto teachings are different from the claimed inventions in that Yamamoto does not disclose or suggest a semiconductor memory that includes control circuitry for selectively varying the data I/O width of a data buffer of the semiconductor memory.

Yamamoto discloses in FIG. 1, for example, a computer system comprising a 32-bit CPU (1) (and other 32-bit devices, e.g., RAM 2), which communicate over a main 32-bit width bus (9) and a plurality of devices (e.g., ROM 5) that are connected to a sub-bus (10) that is less than 32 bits in width (e.g., the sub-bus has a 16 bit width). A gateway (4) is coupled between the high speed 32-bit bus (9) and the sub-bus (10) to control communications of data between the CPU (1) and the ROM (5), etc. (See, Col. 4, lines 10-47).

Yamamoto discloses in FIG. 2, for example, that the gateway (4) includes a data buffer (11) and controller (16) that operate control data communication between the different busses (9) and (10) having different data lengths or bus widths and to synchronize timing of data communication between the CPU (1) and the components (See, Col. 5, lines 5-63).

In formulating the rejections of claims 1, 10, 20, 21, 25, 26 and 27, the Examiner essentially relies on Yamamoto's disclosure of the RAM (2) in FIG. 1 and the data buffer (11) and controller (16) of the gateway (4) illustrated in FIG. 2, contending that such combination of elements teaches a data buffer (11) that stores data written/read to/from the RAM (2), wherein the data width of the data buffer (11) is selectively controlled.

In this regard, however, Yamamoto's teachings are not fairly applicable to the claimed inventions in that Yamamoto is merely concerned with enabling communication between a CPU having a fixed bus width (e.g., 32 bits) and peripheral devices (such as a memory device) having a fixed bus width that is smaller (e.g., 8 bit) than that of the CPU. Yamamoto does not disclose or suggest a memory device having on-chip control circuitry to selectively control the I/O data width of a memory data buffer, as contemplated by the claimed inventions. In fact, Yamamoto teaches that the memories (2) (5), (6) in FIG. 1 are fixed I/O data width (see, e.g., Col. 4, lines 23-41).

Notwithstanding the above, Applicants have amended the claims for the sole purpose of further clarifying the claimed subject matter and the patentable distinctions over the cited art of record. For example, claims 1, 10, 21, 25, 26 and 27 make clear that the data buffers and control circuitry are on-chip components of the memory IC device. Moreover, claim 20 recites *a data width control circuit for selectively varying a data width of the memory data buffer in response to an external control signal applied to one or more address pins of the IC memory device.* Yamamoto clearly does not anticipated the subject matters of claims 1, 10, 20, 21 and 25-27, much less claims 2-6 and 11-15 at least by virtue of their dependence from claims 1 and 10. Accordingly, withdrawal of the anticipation rejections is requested.

Claim Rejections Under 35 U.S.C. §103

Claims 7-9 and 16-19 stand rejected as being unpatentable over Yamamoto and further in view of U.S. Patent No. 4,706,219 to Miyata.

Claims 22-24 stand rejected as being unpatentable over Patterson and AAPA and further in view of U.S. Patent No. 5,349,448 to Hirai.

Given that the above-listed obviousness rejections are based, in part, on the primary reference Yamamoto as applied to the independent claims 1, 10 and 21, it is respectfully submitted that the cited combinations of references are legally deficient to establish a *prima facie* case of obviousness against claims 7-9, 16-19 and 22-24 for *at least* the same reasons given above for claims 1, 10 and 21. Moreover, the cited references Miyata and Hirai clearly do not cure the deficiencies of Yamamoto as noted above with regard to claims 1, 10 and 21. Accordingly, the withdrawal of the obviousness rejections is respectfully requested.

Respectfully submitted,

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